

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Pupplication Serial No 09/536,037
Filing Date March 27, 2000
Inventor
Assignee Micron Technology, Inc.
Group Art Unit
Examiner Toniae M. Thomas
Attorney's Docket No
Title: Low k Interlevel Dielectric Layer Fabrication Methods

## SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed after the filing of the Request for Continued Examination (RCE) Application and before receipt of the first Office Action. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. §1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: 7-16-03

D. Brent Kenady Reg. No. 40,045

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U.S. PATENT DOCUMENTS									
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